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Addendum

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Errata to MPC885 PowerQUICC™ Reference Manual, Rev. 2

This errata describes corrections to the *MPC885 PowerQUICC™ User's Manual,* Revision 2. For convenience, the section number and page number of the errata item in the reference manual are provided. Items in bold are new since the last revision of this document.

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Section, Page No.	Changes
General erratum	Replace all instances of the term ‘60x’ with ‘external.’
10.4.1, 10-4	In Figure 10-2, “Internal Memory Map Register (MMR),” change “PARTNUM” reset from “000_0000” to “0000_1001” or “0x09”.
10.4.1, 10-4	In Figure 10-2, “Internal Memory Map Register (MMR)” and Table 10-2, “MMR Field Descriptions,” change bits 0–15 for ISB to 0–13. Bits 14 and 15 are reserved bits and are restricted to containing only a value of 0 to prevent conflicts between the Internal Memory Map and the SEC's memory map.
12.1.2, 12-22	In Table 12-1, “MPC885/MPC880 Signal Descriptions,” add RMII_MII_MDIO to name column of pin P19.
12.1.2, 12-23	In Table 12-1, “MPC885/MPC880 Signal Descriptions,” add RMII2-TXEN [pin T6] description to MII1-TXEN [pin T5] description.
14.2.1, 14-4	In Table 14-1, “The Input Frequency Requirements,” change “320 MHz” to “400 MHz” as follows:

Table 14-1. The Input Frequency Requirements

MODCK[1-2]	Frequency In	PDF	MFI, MFN, MFD for DPGDCK
00, 01	OSCM = 10 MHz to 10.66 MHz	0	160 MHz < OSCLK × 2 × (MFI + (MFN ÷ (MFD+1))) < 400 MHz
11	EXTCLK = 10 MHz to 10.66 MHz	0	160 MHz < OSCLK × 2 × (MFI + (MFN ÷ (MFD+1))) < 400 MHz
10	45 MHz ≤ EXTCLK ≤ 66 MHz	10 MHz ≤ EXTCLK / (PDF+1) ≤ 32 MHz	160 MHz < OSCLK × 2 × (MFI + (MFN ÷ (MFD+1))) / (PDF+1) < 400 MHz

14.3.1.3, 14-13	In the first bullet note dealing with internal clock of 2 x EXTCLK, add the following: “assuming EXTCLK is between 50 MHz to 80 MHz.”
14.3.3, 14-15	In Table 14-6, “TMBCLK Configuration,” change column heading “MF + 1” to say “MFI/(PDF+1).”
14.4.3, 14-17	In the description, “An inductor value of 8.2 Mhz and bypass capacitor values of 0.1 µF and 10 µF provide a two-pole filter with a cutoff frequency of 500 Hz”, change “8.2 MHz” to “8.2 mH”.
14.6.2, 14-21	In Figure 14-13, “PLL and Reset Control Register (PLPRCR),” change ‘0000’ under field PDF to ‘—’ because PDF is not affected by HRESET.
14.6.2, 14-22	In Figure 14-13, “PLL and Reset Control Register (PLPRCR),” and Table 14-9, “PLPRCR Field Descriptions,” change bit field “FIOPD” to “RESERVED”.
15.6.4.7/15-48	In Table 15-19, “AMA/AMB Definition for DRAM Interface,” add the following footnote to “Memory Size” heading: “Memory size takes data bus width into account.”

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18.6.1, 18-6	In Table 18-4, “RCCR Field Descriptions,” change bit 12 description to say: “EIE. External interrupt enable. Configure as instructed in the download process of a Motorola-supplied RAM microcode package. 0 DREQ0 cannot interrupt the CP. 1 DREQ0 will interrupt the CP. This bit must be set to enable USB host SOF generation.”
18.6.4, 18-9	In Table 18-7, “CP Command Opcodes,” move USB COMMAND from opcode row 1111 to opcode row 1101.
19.1.2, 19-3	In Table 19-1, “U-Bus Arbitration IDs,” change the term ‘G2 Core’ to ‘PTEC Core’.
21.2.4, 21-10	In Table 21-4, “TODR Field Descriptions,” in TOD field description, change “TOD is cleared automatically after one serial clock...” to say “TOD is cleared automatically after 1 system clock...”
27.1, 27-2	In Figure 27-2, “Ethernet Block Diagram,” Clock Generator block: Internal Clock[s] arrows should be reversed; pointing *into* the block, and RCLK and TCLK arrows should be reversed; pointing *out* of the block
31.7.1, 31-9	In Figure 31-5, “USB Controller Operating Modes,” the arrow on the bottom of “Preamble” should point in the opposite direction.
31.7.2, 31-11	In Figure 31-6, “SOF Generation, the “dreq0” signal should point in the opposite direction.
31.7.2, 31-11	In the last paragraph, change to the following: DREQ0 should be configured as external interrupt—bit EIE should be set to 1 in RCCR. When there are no hardware originated requests to the CP, it enters stall state. Configuring DREQ0 as an external interrupt request ensures that only a hardware interrupt request can wake up the host controller.
31.8, 31-12	In Figure 31-7, “USB Parameter RAM Memory Map,” change RSTATE to bold-face type.
31.10, 31-13	In Table 31-4, “Endpoint Parameter Block,” change TSTATE to bold-face type.
31.13.2, 31-28	Modify section to say the following: This command enables the transmission of data from the corresponding endpoint on the USB. This command is expected by the USB controller after a STOP Tx Command, or after transmission error (underrun, time-out, STALL or NAK). To eliminate the USB transmit delay, set STR (start command) in USCOM after launching “RESTART TX” command.”
31.13.2, 31-28	Add the following note to the end of the section: **NOTE** “In Host mode, care should be taken that the RESTART Tx command is not issued during or just before the SOF transmission. To ensure that, the timer’s value can be checked.”

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32.4.3, 32-7	In Table 32-3, “I2BRG Field Descriptions,” change the description for bits 0–7 to read as follows: “Division ratio 0–7. Specifies the divide ratio of the BRG divider in the I^2C clock generator. The output of the prescaler is divided by 2 × (DIV + 3 + (2x FLT)), and the clock has a 50% duty cycle. The FLT bit is in the I2MOD register. The minimum value for DIV is 3 if the digital filter is disabled (FLT = 0) and 6 if the digital filter is enabled (FLT = 1).”
33.8, 33-19	Add a note to beginning of section, as follows: “PIP in transparent mode is not supported.”
34.4.1.4, 34-16	In Figure 34-14, “Port C Special Options Register (PCSO),” change bit 4 to CD3, bit 5 to CTS3, bit 6 to CD4, and bit 7 to CTS4.
35.2.1, 35-3	First bullet should reference SPS = 0 and second bullet should reference SPS = 1.
42.2.2, 42-3	Add the following note below the second paragraph: **NOTE** The actual number of active PHY address signals is selected in UTMODE [ADDPIN]; see Section 43.2, “UTOPIA Mode Register (UTMODE).” When a PHY address signal is not activated, the pin reverts to its function as defined by PBDIR alone (UT becomes a don't care). For example, assuming that the UTOPIA interface has been initialized properly, and if only seven PHYs are used in a UTOPIA master application, the SMC1 data signals are still available because RxAddr [3] and TxAddr [3] are not active.
45.2.1, 45-3	In Table 45-2, “MII and RMII Signals,” add ‘(input)’ next to the signal descriptions ‘Transmit Clock’ and ‘Receive Clock’.
45.2.5, 45-7	In Figure 45-2, “Ethernet Address Recognition Flowchart,” the promiscuous mode check at the bottom should indicate when R_CNTRL[PROM] = 0, the state machine leads to False.
45.3.1, 45-12	Add the following note below Table 45-6, “CPTR RMII Related Field Descriptions”: **NOTE** If auto-negotiation is used, then it is recommended to configure RMIIx_RATE_FECx after the PHY has finished the auto-negotiation. The user can then read the line speed from the PHY status registers using MII management frames, and then configure RMIIx_RATE_FECx accordingly.
45.3.2.13, 45-23	In Figure 45-17, “MII_DATA Register,” remove address offset(s) for FEC_2, 0x1E80 and 0x1E82.
45.3.2.13, 45-24	In the last paragraph, add the following: “In the MPC88x or MPC87x, all MII management interface transactions must be done through FEC1 registers. This includes MII_SPEED and MII_DATA registers.”
45.3.2.14, 45-24	In Figure 45-18, “MII_SPEED Field Descriptions,” remove address offset(s) for FEC_2, 0x1E84 and 0x1E86.

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Appendix F, F-1	Under the first bullet, remove the sentence, “The time-slot assigner is not implemented.”
F.1, F-1	Add “PCMCIA Port A only” to bullet “The MPC875 supports one PCMCIA channel.”
F.2 F, F-2	Add NOTE at end of section:“MPC875 supports PCMCIA Port A only.”
F. 2.2, F-4	Add the following to the list of Other Unimplemented Signals: CE1_B, CE2_B, and ALE_B.

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Europe, Middle East, and Africa:
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Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

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